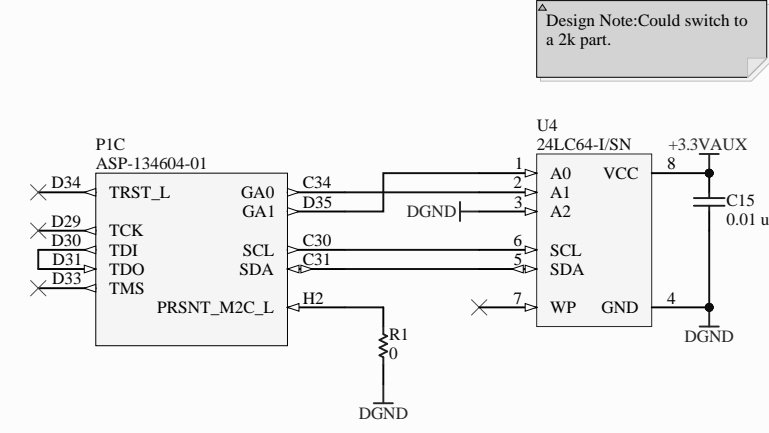


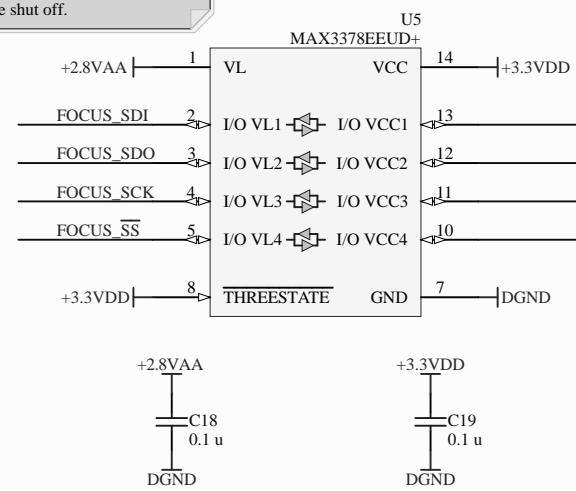
Design Note: Use FX2 clk 48MHz x 2 = 96MHz.

PIA ASP-134604-01	
H4	CLK0_M2C_P
H5	CLK0_M2C_N
G6	LA00_P_CC
G7	LA00_N_CC
D8	LA01_P_CC
D9	LA01_N_CC
H7	LA02_P
H8	LA02_N
G9	LA03_P
G10	LA03_N
H10	LA04_P
H11	LA04_N
D11	LA05_P
D12	LA05_N
C10	LA06_P
D14	LA06_N
C11	LA07_P
H13	LA07_N
H14	LA08_P
G12	LA08_N
G13	LA09_P
D14	LA09_N
D15	LA10_P
C14	LA10_N
C15	LA11_P
H16	LA11_N
H17	LA12_P
G15	LA12_N
G16	LA13_P
D17	LA13_N
D18	LA14_P
C18	LA14_N
H19	LA15_P
H20	LA15_N
G18	LA16_P
G19	LA16_N
D20	LA17_P_CC
D21	LA17_N_CC
C22	LA18_P_CC
H22	LA18_N_CC
H23	LA19_P
G21	LA19_N
G22	LA20_P
H26	LA20_N
H25	LA21_P
G24	LA21_N
G25	LA22_P
D23	LA22_N
D26	LA23_P
D24	LA23_N
H28	LA24_P
H29	LA24_N
G27	LA25_P
G28	LA25_N
D27	LA26_P
C26	LA26_N
C27	LA27_P
H31	LA27_N
H32	LA28_P
G30	LA28_N
G31	LA29_P
H34	LA29_N
H35	LA30_P
G33	LA30_N
G34	LA31_P
H37	LA31_N
H38	LA32_P
G36	LA32_N
G37	LA33_P
G37	LA33_N

PIB ASP-134604-01	
D4	GBTCLK0_M2C_P
D5	GBTCLK0_M2C_N
C6	DP0_M2C_P
C7	DP0_M2C_N
C2	DP0_C2M_P
C3	DP0_C2M_N



Design Note: VL connected to +2.8V instead of Vadj because VL has to be present at all times Vcc is. Vadj can be shut off.



Design Note: VADJ set to 2.5v

