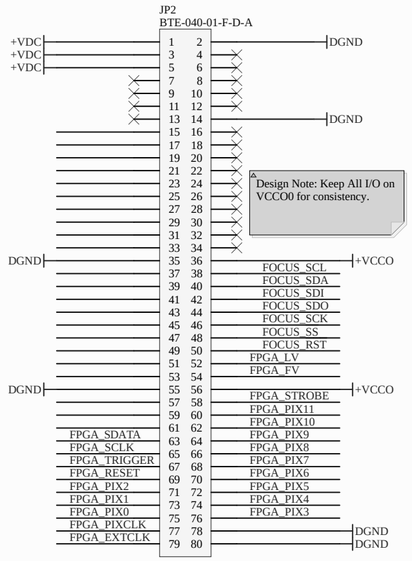
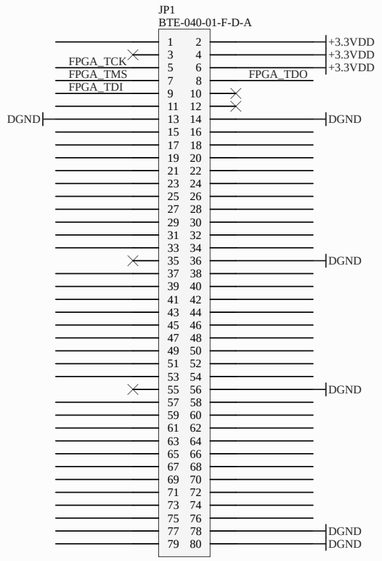
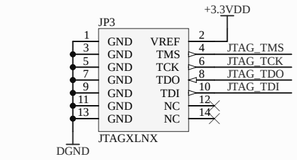
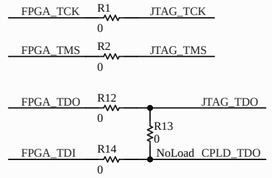
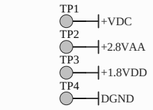
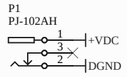






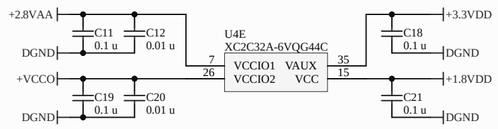


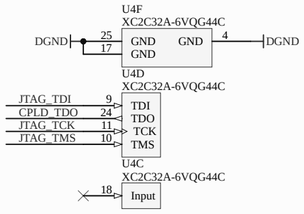


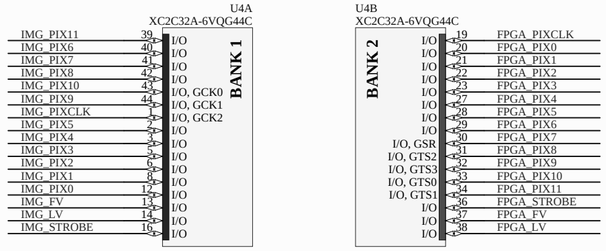


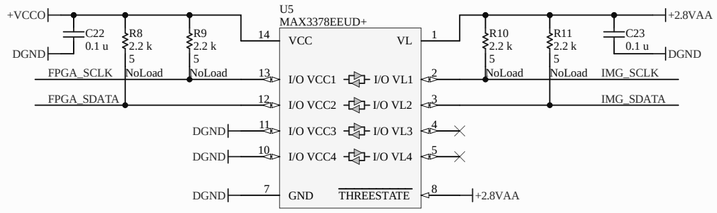
XEM6010 JTAG (default):
+ JTAG_TDI > CPLD_TDI > CPLD_TDO > FPGA_TDI > FPGA_TDO > JTAG_TDO
+ VDD_JTAG == +3.3VDD

XEM3010 JTAG:
+ JTAG_TDI > CPLD_TDI > CPLD_TDO > JTAG_TDO
+ FPGA_TDI and FPGA_TDO disconnected
+ JTAG continuity is not configured

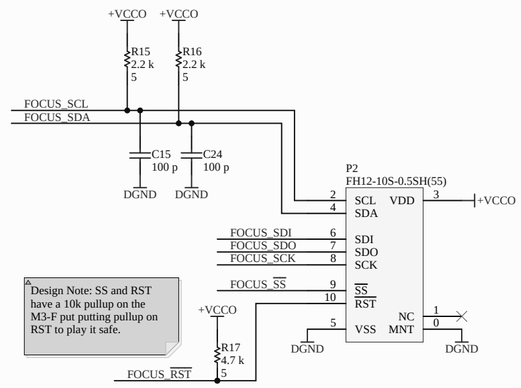




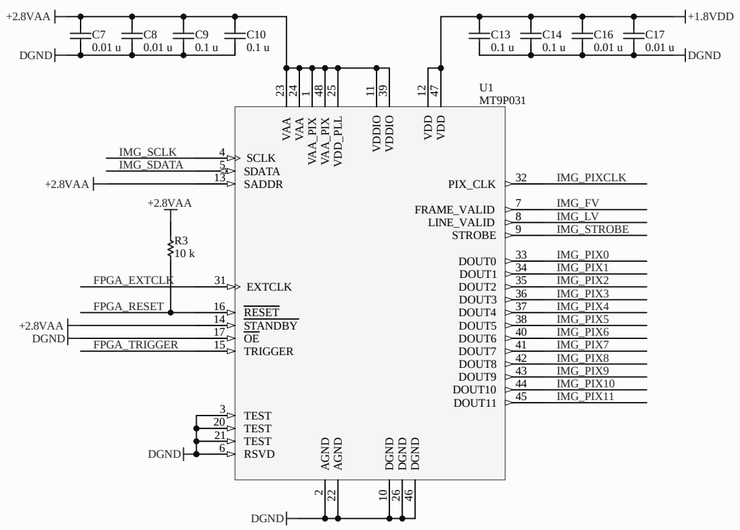


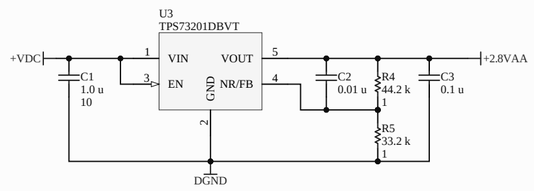


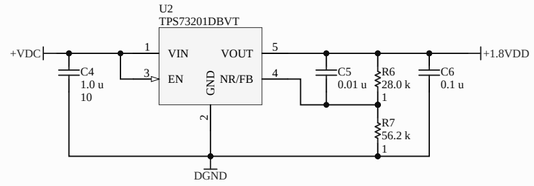
Design Note: Vcco = 3.3V. It must be >2.8V for U5 to work correctly.



Design Note: SS and RST have a 10k pullup on the M3-F put putting pullup on RST to play it safe.







Title	***EVB1005***		
Size: C	Number: xxx	Revision: 2	
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Opal Kelly
13500 SW 72nd Ave, STE 120
Portland, OR 97223
http://www.opalkelly.com

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