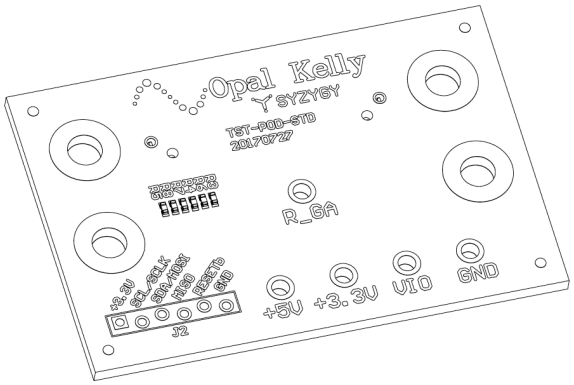
SZG-TST-STD

The SZG-TST-STD is a SYZYGY Standard peripheral intended to be used by SYZYGY carrier developers to test continuity during development or production of their carrier. It can be used during automated testing to validate connector I/O.



Resources

- Aligni PLM - See the **Attachments** tab for schematics and Altium Designer project files.
- SYZYGY Specification

SYZYGY Information

Compatibility Table

Compatibility Parameter	Specification
Port type	SYZYGY Standard
Width	Single
5V supply required	Yes
Nominal 5V supply current	< 10mA
Nominal 3.3V supply current	< 10mA
VIO supply voltage	1.8V
Nominal VIO supply current	< 100mA
Total number of I/O	Up to 28

DNA Data

This data is stored in the SYZYGY DNA microcontroller on the SZG-TST-STD peripheral.

DNA Parameter	Data
Max 5V Load	10 mA
Max 3.3V Load	10 mA
Max VIO Load	10 mA
IS_LVDS	False
IS_DOUBLEWIDE	False
VIO Min	1.8V
VIO Max	1.8V

Pinout

SYZYGY (J1)	Connection

5 (S0)	Atmel PB0 (U1 pin 11)
7 (S2)	Atmel PB1 (U1 pin 12)
9 (S4)	Atmel PB2 (U1 pin 14)
11 (S6)	Atmel PA7 (U1 pin 15)
6 (S1)	8 (S3)
10 (S5)	12 (S7)
13 (S8)	15 (S10)
14 (S9)	16 (S11)
17 (S12)	19 (S14)
18 (S13)	20 (S15)
21 (S16)	23 (S18)
22 (S17)	24 (S19)
25 (S20)	27 (S22)
26 (S21)	28 (S23)
29 (S24)	31 (S26)
30 (S25)	32 (S27)
33 (P2C_CLKp)	35 (P2C_CLKn)
34 (C2P_CLKp)	36 (C2P_CLKn)

Design

The SZG-TST-STD is designed to assist carrier developers perform continuity and power supply tests during development and production testing. To accomplish this, the test peripheral connects a communication path from the FPGA to the Atmel MCU for power supply tests. The remaining pins on the connector are shorted together according to the connections in the table above to allow for continuity testing.

Test Firmware

The Atmel MCU on the test peripherals contains a modified version of the normal DNA firmware. The test firmware removes the power supply sequencing options present in the standard firmware.The test firmware also uses the AVR to measure each of the power supply rails, reporting their status back to the FPGA.

Each supply rail is measured with the internal AVR ADC and checked against a pair of threshold values corresponding to the SYZYGY specified tolerance of that power supply rail. If the supply rail is within its required tolerance the AVR sets a "good" status bit for that rail. The VIO rail is assumed to be at 1.8V by the AVR firmware and the DNA for the test peripheral. A 1.8V VIO is used to maximize compatibility with current FPGA I/O supply requirements.

Supply status is communicated back to the FPGA through SYZYGY pins 5, 7, 9, and 11. The AVR continuously reads AVR pin PA7 (SYZYGY Pin 11 (S6)), then outputs the power supply state on the PB[2:0] pins according to the table below.

		+5V Supply	+3.3V Supply	VIO Supply
PA7 = 1	Good	PB0 = 1	PB2 = 1	PB1 = 1
	Bad	PB0 = 0	PB2 = 0	PB1 = 0
PA7 = 0	Good	PB0 = 0	PB2 = 0	PB1 = 0
	Bad	PB0 = 1	PB2 = 1	PB1 = 1

By toggling the PA7 pin with the FPGA it is possible to test continuity on the MCU pins while also checking the status of each power supply.