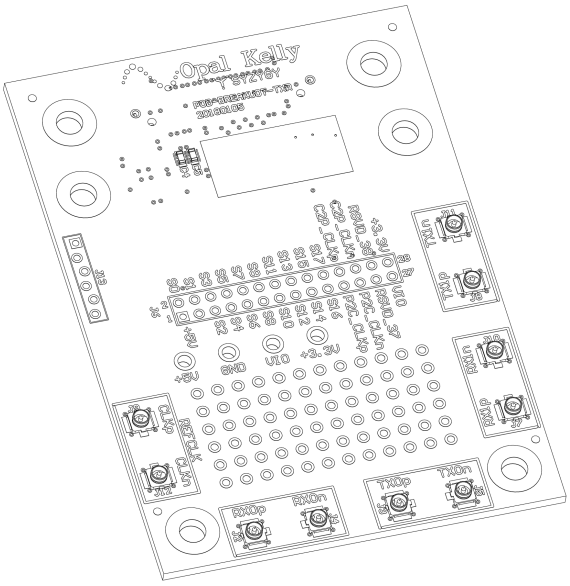
SZG-BRK-TXR

The SZG-BRK-TXR is a SYZYGY Transceiver peripheral intended to be used during early prototype development or experimentation to provide access to the high density SYZYGY ports.

Standard I/O and clocks are pinned out to a 2mm header.

Transceiver pairs are differentially routed on-board and pinned out to paired U.FL connectors at the perimeter.



Resources

- Aligni PLM - See the **Attachments** tab for schematics and Altium Designer project files.
- SYZYGY Specification

SYZYGY Information

Compatibility Table

Compatibility Parameter	Specification
Port type	SYZYGY Transceiver
Width	Single
5V supply required	No
Nominal 5V supply current	N/A
Nominal 3.3V supply current	N/A
VIO supply voltage	1.2V to 3.3V
Nominal VIO supply current	< 100mA
Total number of I/O	Up to 18

DNA Data

This data is stored in the SYZYGY DNA microcontroller on the SZG-BRK-TXR peripheral.

DNA Parameter	Data
Max 5V Load	0 mA
Max 3.3V Load	1000 mA
Max VIO Load	0 mA
IS_LVDS	False
IS_DOUBLEWIDE	False

VIO Min	1.2V
VIO Max	3.3V