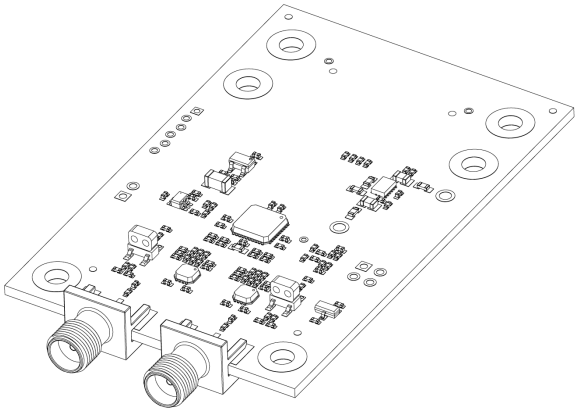
SZG-DAC-AD911X

The SZG-DAC-AD911X is a dual 125 MSPS DAC module featuring the Analog Devices AD9116 TxDAC®. The module is an excellent choice for communication signal paths and general waveform synthesis applications.

In the default configuration, the SMA outputs are ac-coupled through a transformer. With some resistor changes (performed by the end user), a buffered output stage may be selected instead.



Resources

- Aligni PLM - See the **Attachments** tab for schematics and Altium Designer project files.
- SYZYGY Specification
- SYZYGY GitHub Site - Several projects that could be helpful.

SYZYGY Information

Compatibility Table

Compatibility Parameter	Specification
Port type	SYZYGY Standard
Width	Single
5V supply required	Yes
Nominal 5V supply current	200mA
Nominal 3.3V supply current	10mA
VIO supply voltage	1.8V to 3.3V
Nominal VIO supply current	20mA
Total number of I/O	17

DNA Data

This data is stored in the SYZYGY DNA microcontroller on the SZG-DAC-AD911X peripheral.

DNA Parameter	Data
Max 5V Load	200 mA
Max 3.3V Load	10 mA
Max VIO Load	20 mA
IS_LVDS	False
IS_DOUBLEWIDE	False
VIO Min	1.8V
VIO Max	3.3V

Pinout

SYZYGY (J1)	Connection	Note
5 (S0)	DAC DB0	
6 (S1)	DAC DB1	
7 (S2)	DAC DB2	
8 (S3)	DAC DB3	
9 (S4)	DAC DB4	
10 (S5)	DAC DB5	
11 (S6)	DAC DB6	
12 (S7)	DAC DB7	
13 (S8)	DAC DB8	
14 (S9)	DAC DB9	
15 (S10)	DAC DB10	
16 (S11)	DAC DB11	
17 (S12)	DAC CS_B/PWRDN	
18 (S13)	DAC SCLK/CLKMD	
19 (S14)	DAC SDIO/FORMAT	
20 (S15)	OPAMP_ENABLE	Assert (1) to enable both DAC I and DAC Q outputs. Deassert (0) to place both op-amps in power-down.
21 (S16)	DAC RESET/PINMD	
33 (P2C_CLKp)	DAC DCLKIO	Optional clock output (See schematics and DAC datasheet)
34 (C2P_CLKp)	DAC CLKIN	Input clock to DAC through CLKIN level translator (U3)

Design

The design of the SZG-DAC-AD911X has been heavily influenced by the evaluation board designed and produced by Analog Devices. You might find it interesting to note that we sell the SZG-DAC-AD911X for significantly less than Analog Devices sell their eval board through Digi-Key (AD9116-DPG2-EBZ-ND).

Analog Devices ADA4857

From the Analog Devices datasheet:

> The AD9114/AD9115/AD9116/AD9117 are pin-compatible dual, 8-/10-/12-/14-bit, low power digital-to-analog converters (DACs) that provide a sample rate of 125 MSPS. These TxDAC® converters are optimized for the transmit signal path of communication systems. All the devices share the same interface, package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost.
>
> The AD9114/AD9115/AD9116/AD9117 offer exceptional ac and dc performance and support update rates up to 125 MSPS.
>
> The flexible power supply operating range of 1.8 V to 3.3 V and low power dissipation of the AD9114/AD9115/AD9116/AD9117 make them well suited for portable and low power applications.

Output Stage

By default, the SZG-DAC-AD911X is configured to provide single-ended, transformer-coupled outputs to SMA connectors J2 and J4. To use the buffered output stage instead, remove resistors R25, R27, R74, and R78, and place resistors R7, R13, R53, and R60.

The bias networks for doth output stages may be configured for specific applications. Refer to the documentation below.

Auxiliary Output

By default, the SZG-DAC-AD911X is configured to use the AD911X internal full-scale current adjust capability. In this configuration, the FSADJx/AUXx pins may be used as auxiliary DAC outputs. On the SZG-DAC-AD911X these outputs are provided on header J6. Refer to the documentation below for more information on using the auxiliary DAC outputs.

Clock Input

By default, the SZG-DAC-AD911X is configured to accept a single-ended CMOS clock over the C2P_CLKp connection from the carrier. In this configuration, the clock signal from the carrier is applied to the CLKIN and DCLKIO pins on the AD911x. If DCLKIO is configured as an output, remove R39 and place R34 -- this connects DCLKIO to the P2C_CLKp pin for use on the carrier.

To apply an external clock source at J3, remove R39, R46, and R47. To apply the external clock to the DCLKIO pin, place R43. To connect the DCLKIO signal to the carrier at pin P2C_CLKp, place R34.

Additional Documentation

Analog Devices AD9116 data sheet
http://www.analog.com/en/products/digital-to-analog-converters/standard-dac/high-speed-da-converters/ad9116.html

Analog Devices AD9116 evaluation board EVAL-AD9116
http://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/EVAL-AD9116.html