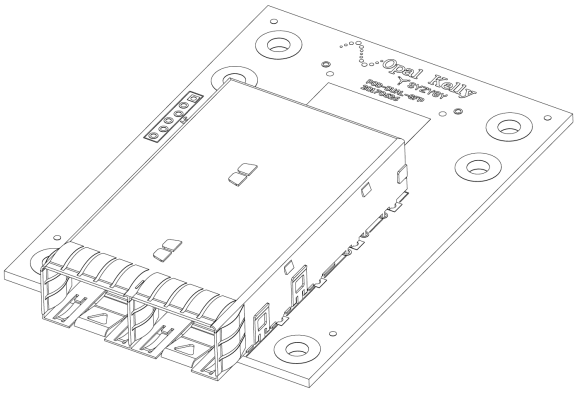
SZG-DUALSFP

The DUALSFP peripheral provides a pair of SFP+ sockets to a SYZYGY Transceiver port for use with high-performance serial standards over optical or copper wire connections.



Resources

- Aligni Reference (username:`syzygy-public@opalkelly.com` / password:`syzygy`)
- SYZYGY Specification

SYZYGY Information

Compatibility Table

Compatibility Parameter	Specification
Port type	SYZYGY Transceiver
Width	Single
5V supply required	No
Nominal 5V supply current	N/A
Nominal 3.3V supply current	360 mA (based on 2x Finisar FTLF8524P2BNV modules)
VIO supply voltage	3.3V
Nominal VIO supply current	< 100mA
Total number of I/O	14

DNA Data

This data is stored in the SYZYGY DNA microcontroller on the SZG-DUALSFP peripheral.

Note that the maximum 3.3V load below is an overestimate due to the variability in power consumption between SFP modules.

DNA Parameter	Data
Max 5V Load	0 mA
Max 3.3V Load	2000 mA
Max VIO Load	10 mA
IS_LVDS	False
IS_DOUBLEWIDE	False
VIO Min	3.3V
VIO Max	3.3V

Pinout

SYZYGY (J1)	Connection	Note
5 (RX0p)	SFP1_RDP	
7 (RX0n)	SFP1_RDN	
6 (TX0p)	SFP1_TDP	
8 (TX0n)	SFP1_TDN	
9 (RX1p)	SFP2_RDP	
11 (RX1n)	SFP2_RDN	
10 (TX1p)	SFP2_TDP	
12 (TX1n)	SFP2_TDN	
13 (REFCLKp)	REFCLKP	125 MHz LVDS clock
15 (REFCLKn)	REFCLKN	125 MHz LVDS clock
14 (S0)	SFP1_MOD_DEF2	
16 (S1)	SFP1_RATE_SELECT	
17 (S2)	SFP1_TFAULT	
18 (S3)	SFP2_TDIS	
19 (S4)	SFP1_TDIS	
20 (S5)	SFP2_MOD_DEF2	
21 (S6)	SFP1_MOD_DEF1	
22 (S7)	SFP2_MOD_DEF1	
23 (S8)	SFP1_MOD_DEF0	
24 (S9)	SFP2_MOD_DEF0	
25 (S10)	SFP1_LOS	
26 (S11)	SFP2_RATE_SELECT	
27 (S12)	SFP2_TFAULT	
28 (S13)	SFP2_LOS	

Design

The DUALSFP peripheral provides a pair of SFP+ sockets to a SYZYGY Transceiver port for use with high-performance serial standards over optical or copper wire connections.

Primary Components

Component	Manufacturer	Manufacturer P/N
Dual SFP Cage	Amphenol	U77-A2114-200T
SFP Receptacle	Amphenol	UE75-A20-6000T

Tested SFP Modules

Manufacturer	Manufacturer P/N	Comment
Finisar	FTLF8524P2BNV	4.25 Gb/s Short-Wavelength SFP Transceiver

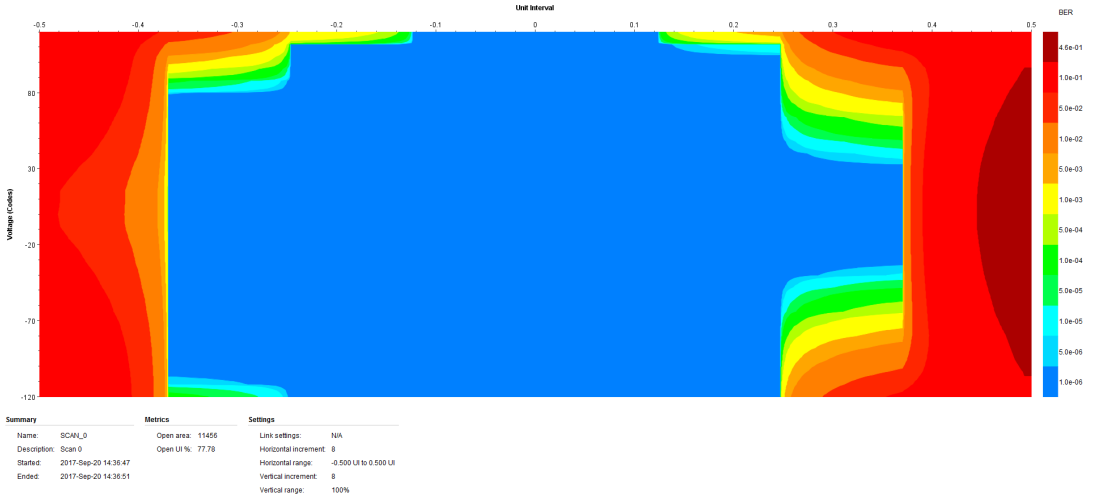
Eye Diagrams

Several eye diagrams were taken using Xilinx's iBERT tool to empirically test the quality of the link.

Test conditions and setup:

- Vivado 2017.2
- iBERT version 3.0 (Rev. 15)
- Brain-1 used as the carrier
- Peripheral contained two Finisar FTL8524P2BNV SFP transceivers
- Scans performed at 3.75Gbps

Scan 0 (SFP1 Position - Direct SYZYGY)



Scan 1 (SFP2 Position - Direct SYZYGY)