Pins

Opal Kelly Pins is an interactive online reference for the expansion connectors on all Opal Kelly FPGA integration modules. It provides additional information on pin capabilities, pin characteristics, and PCB routing. Additionally, Pins provides a tool for generating constraint files for place and route tools. Pins can be found at the URL to the right.

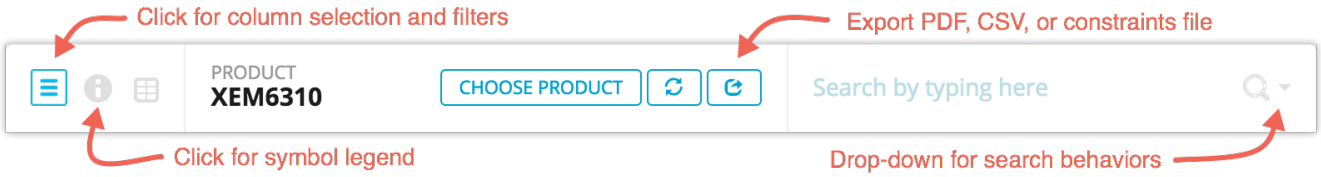
Pin lists are currently available for the following products:

XEM3001	XEM3005	XEM3010	XEM3050
XEM5010	XEM6001	XEM6002	XEM6006
XEM6010	XEM6310	XEM6310MT	XEM7001
XEM7010	XEM7310	XEM7320	XEM7350
XEM7360	ZEM4310	ZEM5305	ZEM5310
Brain-1			

Pins Home

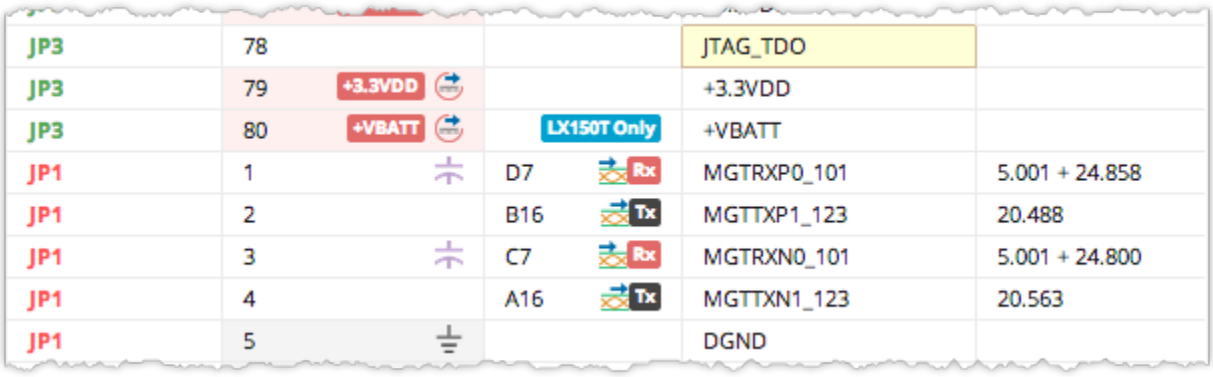
Toolbar

The toolbar at the top of a Pins product page has a number of features. Explore a bit; you won't break it.



Presentation

Each product's Pin List is presented in table form with one row representing a single pin on one of the expansion connectors. The cells within the row contain various information associated with that pin such as connector reference designator, pin number, the FPGA location routed to the pin, routed length, and other attributes. A number of standard symbols are used to represent qualities of a pin such as the presence of ac-coupling, the I/O functionality of the pin, or power connections. A legend describing these symbols is available by clicking an icon at the top left of the Pin List.



Exporting a Pin List or Constraints File

Click **Export as CSV** to save a CSV version of the Pin List which can be loaded into a spreadsheet for further manipulation offline. All columns, including filterable columns which are not necessarily displayed in the Pin List are exported to the CSV.

Click **Export as PDF** to generate a PDF containing the filtered Pin List for printing.

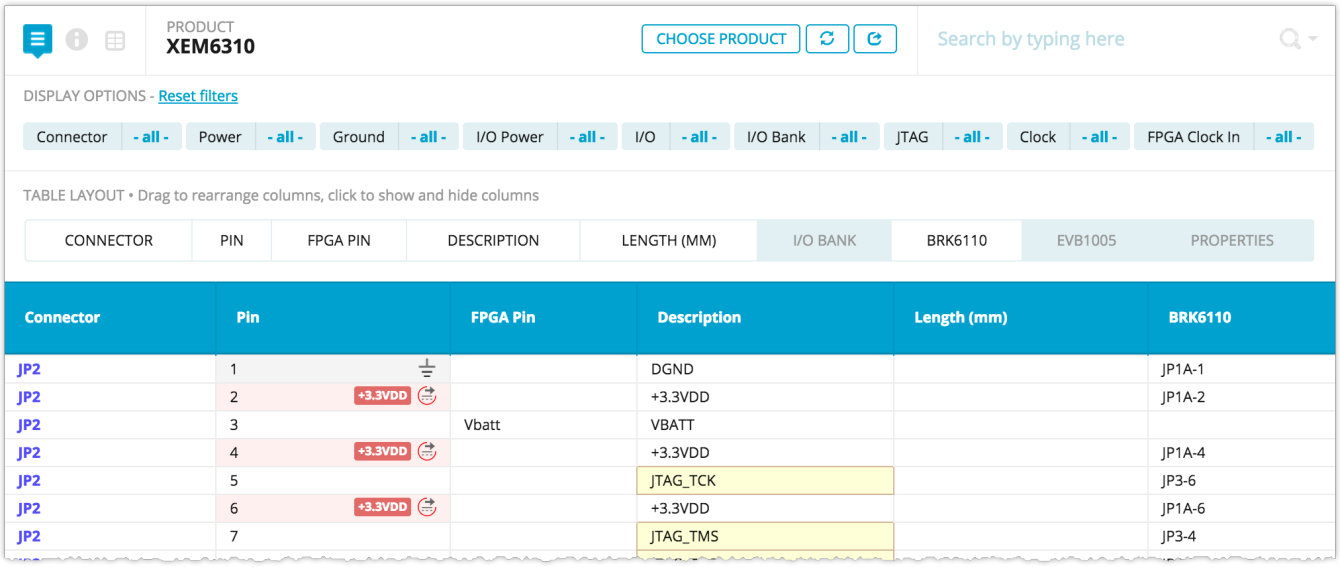
Click **Generate Constraints File** to generate a template UCF file for the device. The constraints file will contain a comprehensive list of all expansion connector FPGA pins and all additional device features.

> ⚠ We have tried to capture significant FPGA pin capabilities in the Pin List. However, the FPGA Datasheet should be used as the authority on pin capabilities and design considerations.

Pin Lists

As the primary reference for Opal Kelly integration module expansion connectors, Pin Lists contain a comprehensive table of the FPGA-to-Connector data including connector pin, FPGA pin, signal description, routed length (when applicable), breakout board pin mapping, FPGA I/O bank, and other properties.

By default, not all data columns are visible. Click on the “Toggle Filters” icon at the top-left to select which columns to show. Depending on the specific module, several additional columns may be shown. The data in these columns is always exported when you export the pin list to CSV.



Search

You can search the pin list using the search entry at the top-right. Click on the magnifying glass drop-down to adjust the function of the search to one of:

- **Highlight** - Highlights search results only.
- **Hide Matching** - Hides rows where search matches are found.
- **Show Only Matching** - Shows only rows where a search match is found.

Table Customization

A number of customizations are available by expanding the Display Options panel at the top of the Pin List. The available table columns may be reordered by dragging their respective tab to a new location or individually enabled / disabled by clicking on the tab.

Note that we have designated some of the available columns as “disabled” by default to focus attention on the most commonly used information.

View Density

Also near the Display Options button is a “Table Layout” button that toggles the table cell density between two settings.

Filters

Each pin list has several properties defined for each pin. The Display Options panel has a list of these properties which can be used to filter displayed pins for easier navigation and project definition. When a specific attribute value is selected, Pins will display only those device pins that match the attribute value.

Filters can be used to quickly identify groups of pins that fit a particular purpose. For example, most Pin Lists have a boolean property called “FPGA I/O” that is set to **true** for any connector pin that is routed to an available I/O on the FPGA. Filtering on this property removes all expansion pins that are not I/Os, allowing you to focus on available connections for your design.

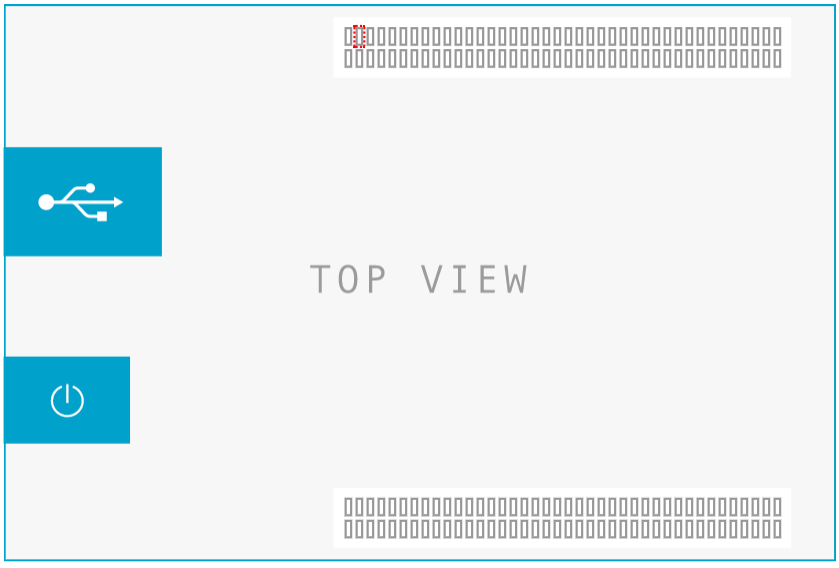
Search

Pins search capability is implemented with three different modes that define the behavior when the search string is found.

- **Highlight only** – Search matches are highlighted in yellow in the table cells.
- **Hide matched** – When search text is found in a row, that row is hidden from view.
- **Show only matched** – Only rows that contain the search text are shown. Other rows are hidden from view.

Pin Diagrams

Pin Diagrams can help you identify the location of pins on the module. To open the pin diagram for a Pin List, click on any of the rows in the list. The diagram will appear in a section at the top of the page. As you hover over pin list table rows, the corresponding pin in the diagram will highlight.



Peripherals

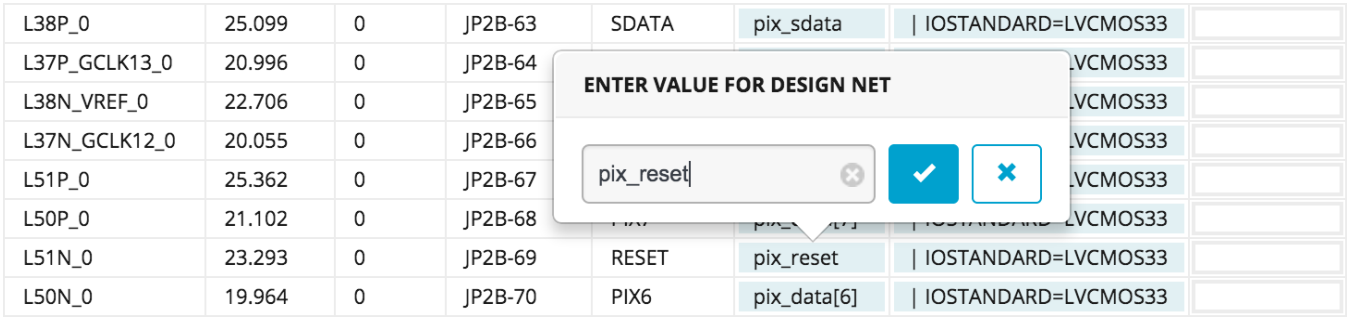
A Peripheral is a user-defined set of signal names that associate to the pins on a pin list. Peripherals help you define the expansion pinout for your attached device and HDL design. Pins can automatically generate the constraint file used in Xilinx and Altera place and route tools based on the Pins source data and your peripheral.

Creating a New Peripheral

Create a new Peripheral by clicking “New Peripheral” on the Peripherals List, then select a Pin List that will define the Peripheral and add a name and description to identify the Peripheral. After you’ve created the Peripheral, you’ll be able to define more details about how constraints files will be generated.

Design Entries

Each Pin List has at least one column that may be used to specify additional information for some pins. For example, the column “Design Net” represents the name of a signal net within your FPGA HDL design that is associated to an external pin. This is required for FPGA pin location mapping within the constraint file. These user columns are not visible on the Pin List, but they contain editable fields that are stored with the Peripheral and exported to the Constraint File as needed.



L38P_0	25.099	0	JP2B-63	SDATA	pix_sdata	| IOSTANDARD=LVCMOS33
L37P_GCLK13_0	20.996	0	JP2B-64			LVCMOS33
L38N_VREF_0	22.706	0	JP2B-65			LVCMOS33
L37N_GCLK12_0	20.055	0	JP2B-66			LVCMOS33
L51P_0	25.362	0	JP2B-67			LVCMOS33
L50P_0	21.102	0	JP2B-68			LVCMOS33
L51N_0	23.293	0	JP2B-69	RESET	pix_reset	| IOSTANDARD=LVCMOS33
L50N_0	19.964	0	JP2B-70	PIX6	pix_data[6]	| IOSTANDARD=LVCMOS33

Specifying Net Names

The Pin List view for a Peripheral includes three additional, editable columns:

- **Design Net** - The name of the signal as it appears in your top-level HDL.
- **Constraints** - Text that is inserted into the constraints file for that signal.
- **Comment** - Additional comment text that is added to the constraints file.

These additional data are merged with the default Pin List constraints file prior to export. The result is a constraints file complete with net names that can be used with your FPGA development flow.

Constraint File Generation (UCF / QSF)

One of the primary motivations for the Peripherals feature is the automatic generation of Xilinx and Altera constraint files, known as “UCF” (Xilinx) or “QSF” (Altera) files. These files are used by the place and route tools to assign signal nets to particular pin locations on the FPGA package. Correspondingly, they are how signal nets get mapped to specific pins on the integration module. Automating this process through Pins greatly simplifies the process of mapping the signals in your HDL to pins on the module.

Click on “Generate Constraints File” from the Peripheral Editor (or the Peripheral List) at any time to generate the constraint file.

Selecting Module Features
In addition to the expansion connections, Opal Kelly FPGA integration modules contain other features such as pushbuttons, LEDs, memory, and the FrontPanel host interface. Depending on your application, you may want to include the constraints for one or more of these additional features in your constraints file. You can enable or disable each feature by editing the Peripheral Details.

In addition to the standard features, we’ve provided user-definable **Lead In** and **Lead Out** sections. Add your own constraints to these sections and Pins will insert them into the generated constraints file.

Export Features

Enable the specific module features you would like to
appear in the exported constraints file. When a feature is enabled, Pins will export the constraints appropriate to that feature such as pin locations. When a feature is disabled, Pins will skip that portion.

The User Lead In and User Lead Out sections allow you to add custom payloads (your own constraints) that will be added to the exported constraints file. Additional timing constraints or comments can be added here.

Constraint file template	Default
Output filename	xem6310.ucf
Export features	☑ Lead In ☑ FrontPanel ☑ FrontPanel Timing ☐ System Clock ☐ Reset ☐ User Lead In Add payload ☑ LEDs ☐ FPGA Flash ☑ DDR2 ☐ User Lead Out Add payload